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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/733,418	12/08/2000	Salman Akram	96-0841.01	6082

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EXAMINER	
BROCK II, PAUL E	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/733,418	AKRAM, SALMAN	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-43 and 45-56* is/are pending in the application.

4a) Of the above claim(s) *32,39,42,45-49 and 55* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-31,33-38,40,41,43,50-54 and 56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Claims 32, 39, 42, 45 – 49 and 55 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 5.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 50, 52 – 54, and 56 are rejected under 35 U.S.C. 102(b) as being anticipated by Wu (USPAT 5393692).

With regard to claim 50, Wu discloses in figures 8 – 11b forming a trench (54) into a semiconductor substrate (20). Wu discloses in figures 8 – 11b forming a single layer dielectric lining (55) on the surface of the trench. Wu discloses in figures 8 – 11b forming a semiconductive spacer (58) along the sidewall of the trench over and in direct contact with the single layer dielectric lining. Wu discloses in figures 8 – 11b forming substantially uniform insulative material (63) in the trench at least partially by substantially consuming the

semiconductive spacer and the single layer dielectric lining to substantially fill the trench with the substantially uniform insulative material without forming a diffusion region at the base of the trench.

With regard to claim 52, Wu discloses in figures 8 – 11b further comprising the step of forming an insulation layer (22) on the semiconductor substrate prior to the step of forming a first trench.

With regard to claim 53, Wu discloses in figures 8 – 11b annealing the semiconductor assembly in the presence of an oxidizing agent.

With regard to claim 54, Wu discloses in figures 8 – 11b wherein the insulative material and the dielectric lining are the same material.

With regard to claim 56, Wu discloses in figures 8 – 11b wherein the process uses only one mask (28) to form the device isolation.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 25, 27 – 31, 33, 34, 36 – 38, 40, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu in view of Kameyama (USPAT 4472240).

With regard to claim 25, Wu discloses in figures 8 – 11b forming a first trench into a semiconductor substrate. Wu discloses in figures 8 – 11b forming a single layer dielectric lining on the surface of the first trench. Wu discloses in figures 8 – 11b forming a spacer along the sidewall of the first trench over and in direct contact with the single layer dielectric lining. Wu discloses in figures 8 – 11b forming an insulative material in the first trench at least partially by substantially consuming the spacer and the single layer dielectric lining to substantially fill the first trench with the insulative material without forming a diffusion region at the base of the trench. Wu does not teach forming a second trench into the substrate assembly at the bottom of the first trench while using the spacer as an etching guide. Kameyama teaches in figure 4e forming a second trench (107) into the semiconductor substrate at the bottom of a first trench (104) by using a spacer (106a and 106b) as an etching guide. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the etching of the second trench of Kameyama in the method of Wu in order to form an element isolation region in a self-aligned manner with excellent controllability without forming a cavity therein as stated by Kameyama in column 2, lines 51 – 55. Kameyama also teaches in column 4, lines 18 – 25 forming an insulative material in the first and second trenches substantially filling the first and second trenches with the insulative material without forming a diffusion region at the base of the second trench. Therefore, it would further have been obvious to combine the method of filling the trenches of Wu and Kameyama.

With regard to claim 27, Wu discloses in figures 8 – 11b wherein the spacer is formed from an oxidizable material.

With regard to claim 28, Kameyama discloses in column 3, lines 60 – 68 wherein the spacer is formed of oxide.

With regard to claim 29, Wu discloses in figures 8 – 11b further comprising the step of forming an insulation layer on the semiconductor substrate prior to the step of forming a first trench.

With regard to claim 30, Wu discloses in figures 8 – 11b annealing the semiconductor assembly in the presence of an oxidizing agent.

With regard to claim 31, Wu discloses in figures 8 – 11b wherein the insulative material and the dielectric lining are the same type material.

With regard to claim 33, Wu discloses in figures 8 – 11b wherein the process uses only one mask to form the device isolation.

With regard to claim 34, Wu discloses in figures 8 – 11b forming a first trench into a semiconductor substrate. Wu discloses in figures 8 – 11b forming a single layer dielectric lining on the surface of the first trench. Wu discloses in figures 8 – 11b forming a semiconductive spacer along the sidewall of the first trench over and in direct contact with the single layer dielectric lining. Wu discloses in figures 8 – 11b forming a substantially uniform insulative material in the first trench at least partially by substantially consuming the semiconductive spacer and the single layer dielectric lining during formation to substantially fill the first trench with the substantially uniform insulative material without forming a diffusion at the base of the trench. Wu does not teach forming a second trench into the semiconductor substrate assembly at the bottom of the first trench while using the spacer as an etching guide. Kameyama teaches in figure 4e forming a second trench (107) into the semiconductor substrate at the bottom of a first

trench (104) by using a spacer (106a and 106b) as an etching guide, the semiconductor substrate being devoid of a bordering diffusion region at the base of the second trench. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the etching of the second trench of Kameyama in the method of Wu in order to form an element isolation region in a self-aligned manner with excellent controllability without forming a cavity therein as stated by Kameyama in column 2, lines 51 – 55. Kameyama also teaches in column 4, lines 18 – 25 forming an oxide filler in the first and second trenches substantially filling the first and second trenches without forming a diffusion at the base of the trench. Therefore, it would further have been obvious to combine the method of filling the trenches of Wu and Kameyama. Wu discloses in figures 8 – 11b planarizing the insulative material. Wu discloses in figures 8 – 11b wherein the process uses only one mask to form the device isolation.

With regard to claim 36, Wu discloses in figures 8 – 11b further comprising the step of forming an insulation layer on the semiconductor substrate prior to the step of forming a first trench.

With regard to claim 37, Wu discloses in figures 8 – 11b annealing the semiconductor assembly in the presence of an oxidizing agent.

With regard to claim 38, Wu discloses in figures 8 – 11b wherein the insulative material and the single layer dielectric lining are the same type material.

With regard to claim 40, Wu discloses in figures 8 – 11b forming a first mask over a silicon substrate assembly. Wu discloses in figures 8 – 11b forming a first trench into the silicon substrate assembly using the mask as an etching guide. Wu discloses in figures 8 – 11b forming an oxide layer on the surface of the first trench. Wu discloses in figures 8 – 11b forming a

silicon spacer on the sidewall of the first trench over and in direct contact with the single layer dielectric lining. Wu discloses in figures 8 – 11b forming an oxide filler substantially devoid of other constituents in the first trench at least partially by substantially consuming the silicon spacer and the oxide layer to substantially fill the first trench with the oxide filler without forming a diffusion region at the base of the trench. Wu does not disclose forming a second trench into the semiconductor substrate assembly at the bottom of the first trench while using the spacer as an etching guide. Kameyama teaches in figure 4e forming a second trench (107) into the semiconductor substrate assembly at the bottom of a first trench (104) by using a spacer (106a and 106b) as an etching guide. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the etching of the second trench of Kameyama in the method of Wu in order to form an element isolation region in a self-aligned manner with excellent controllability without forming a cavity therein as stated by Kameyama in column 2, lines 51 – 55. Kameyama also teaches in column 4, lines 18 – 25 forming an oxide filler in the first and second trenches substantially filling the first and second trenches without forming a diffusion region at the base of the second trench. Therefore, it would further have been obvious to combine the method of filling the trenches of Wu and Kameyama. Wu discloses in figures 8 – 11b planarizing the oxide filler.

With regard to claim 43, Wu discloses in figures 8 – 11b annealing the semiconductor assembly in the presence of an oxidizing agent.

6. Claim 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu as applied to claim 50 above, and further in view of Thomas et al. (USPAT 4922318, Thomas).

With regard to claim 51, Wu discloses in column 1, lines 7 – 22 individual device structures. Typically these individual device structures comprise diffusion regions. Wu does not teach wherein an overall depth of the trench is two times a depth of a bordering diffusion region. Thomas discloses in figure 6 an overall depth of a trench (22) is two times a depth of a bordering diffusion region (84a). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the depth relationship of Thomas in the method of Wu in order to ensure adequate isolation between neighboring active areas which comprise device structures.

7. Claims 26, 35, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu and Kameyama as applied to claims 25, 34, and 40 above, and further in view of Thomas.

Wu discloses in column 1, lines 7 – 22 individual device structures. Typically these individual device structures comprise diffusion regions. Wu does not teach wherein an overall depth of the first trench is two times a depth of a bordering diffusion region. Thomas discloses in figure 6 an overall depth of a trench (22) is two times a depth of a bordering diffusion region (84a). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the depth relationship of Thomas in the method of Wu and Kameyama in order to ensure adequate isolation between neighboring active areas which comprise device structures.

Response to Arguments

8. Applicant's arguments with respect to claims 25 – 31, 33 – 38, 40, 41, 43, 50 – 54, and 56 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
June 11, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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